



Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

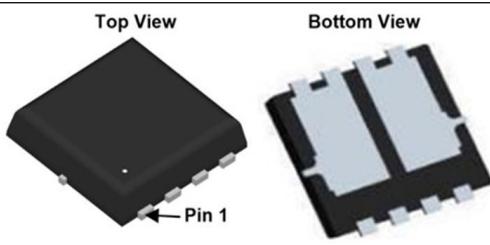
- 30V,22A
 $R_{DS(ON)} < 13\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
 $R_{DS(ON)} < 19\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Application

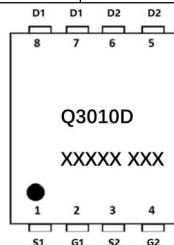
- Load Switch
- PWM Application
- Power Management



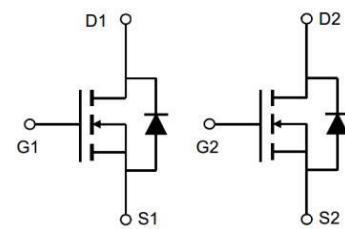
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN3x3-8L-D



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel (pcs)	Per Carton (pcs)
Q3010D	JMTQ3010D	TAPING	PDFN3x3-8L-D	13"	5000	50000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_c = 25^\circ\text{C}$	22	A
		$T_c = 100^\circ\text{C}$	14	A
I_{DM}	Pulsed Drain Current ^{note1}		88	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		24	mJ
P_D	Power Dissipation	$T_c = 25^\circ\text{C}$	9.8	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		12.8	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}= \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}$, $I_D=15\text{A}$	-	10	13	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$	-	14	19	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	1011	-	pF
C_{oss}	Output Capacitance		-	142	-	pF
C_{rss}	Reverse Transfer Capacitance		-	119	-	pF
Q_g	Total Gate Charge	$V_{DD}=15\text{V}$, $I_D=10\text{A}$, $V_{GS}=10\text{V}$	-	19	-	nC
Q_{gs}	Gate-Source Charge		-	6.3	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	4.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}$, $I_D=20\text{A}$, $R_{\text{GEN}}=3\Omega$, $V_{GS}=10\text{V}$	-	6	-	ns
t_r	Turn-on Rise Time		-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	25	-	ns
t_f	Turn-off Fall Time		-	7	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	22	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	88	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s=22\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=10\text{A}$, $di/dt=100\text{A}/\mu\text{s}$	-	7	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	6.3	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: Starting $T_J=25^\circ\text{C}$, $V_{GS}=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=9.8\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

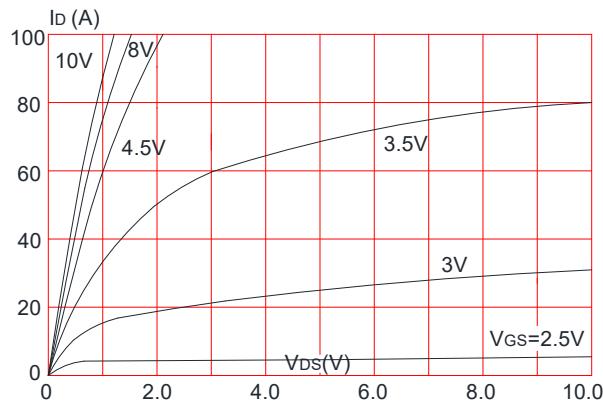


Figure 3: On-resistance vs. Drain Current

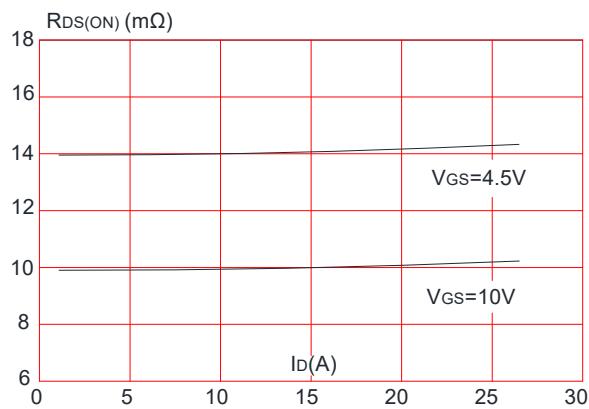


Figure 5: Gate Charge Characteristics

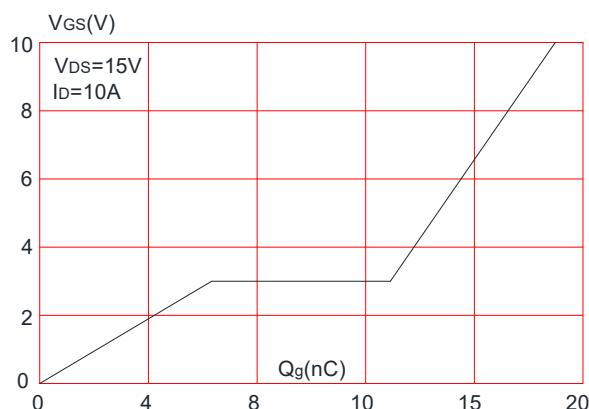


Figure 2: Typical Transfer Characteristics

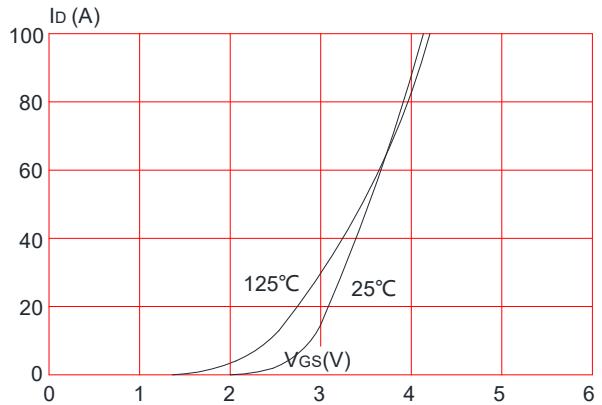


Figure 4: Body Diode Characteristics

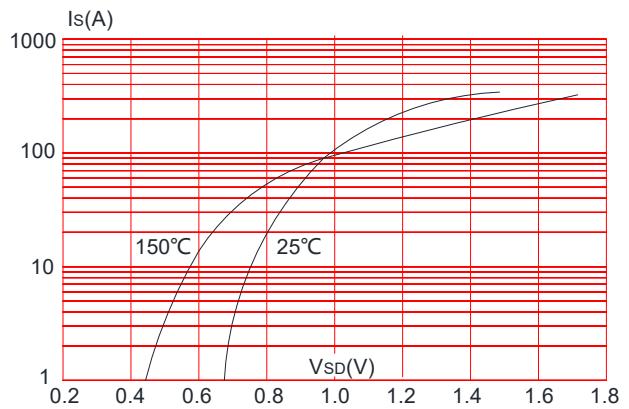


Figure 6: Capacitance Characteristics

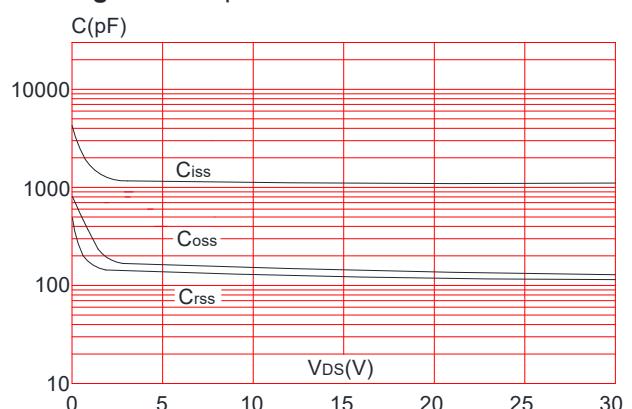


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

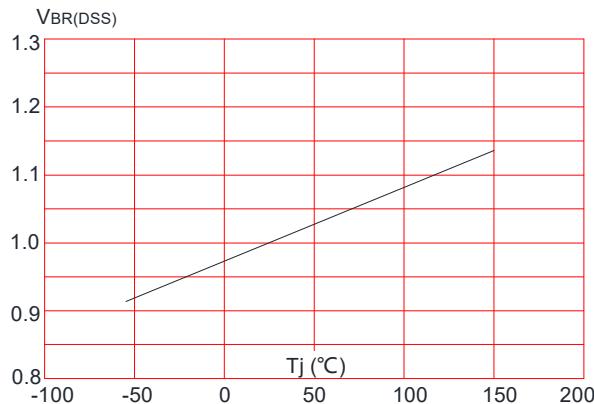


Figure 9: Maximum Safe Operating Area

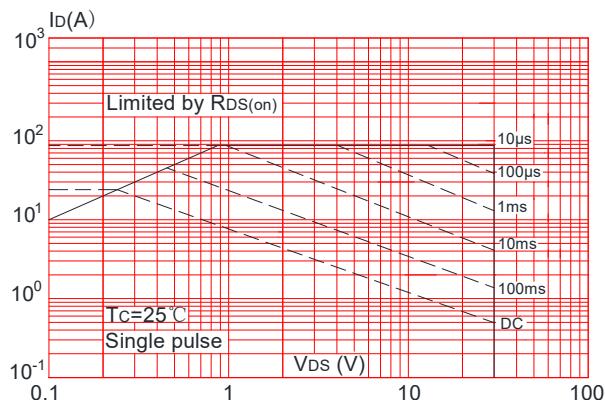


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

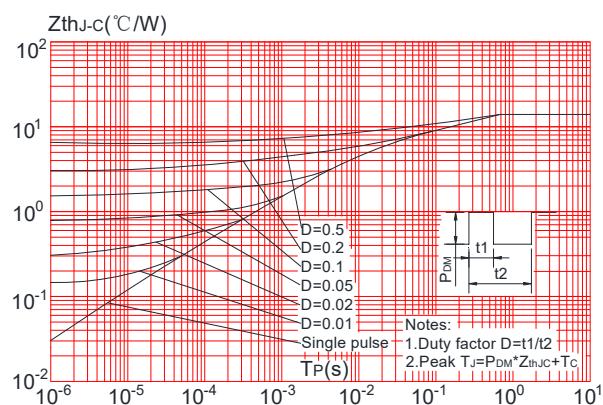


Figure 8: Normalized on Resistance vs. Junction Temperature

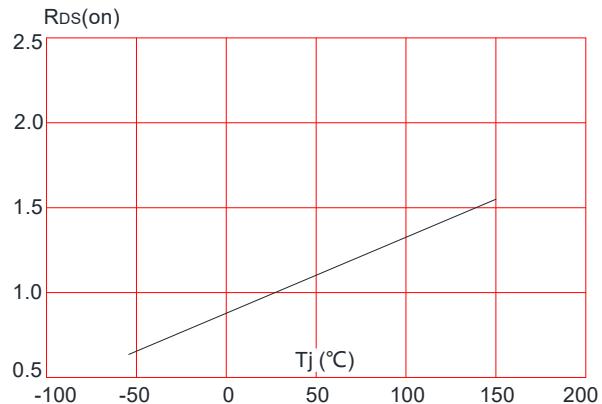
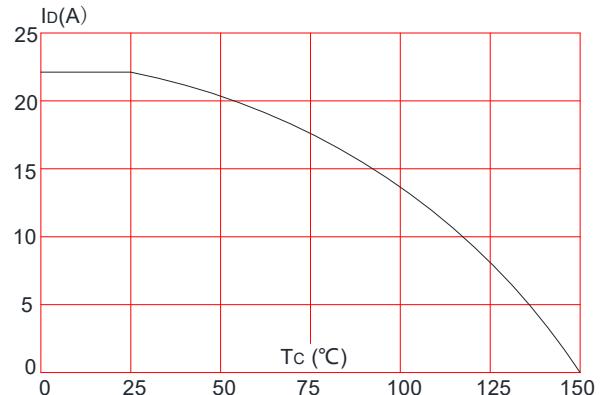


Figure 10: Maximum Continuous Drain Current vs. Case Temperature



Test Circuit

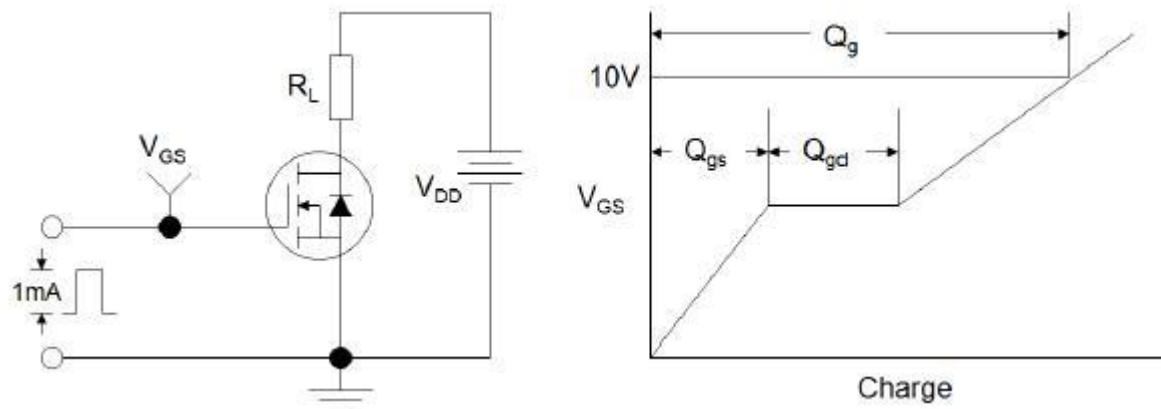


Figure1:Gate Charge Test Circuit & Waveform

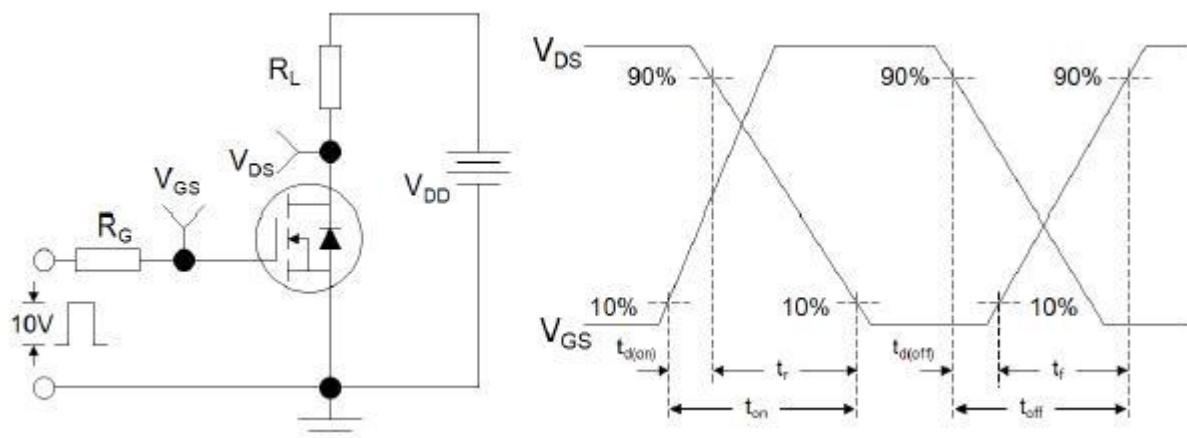


Figure 2: Resistive Switching Test Circuit & Waveforms

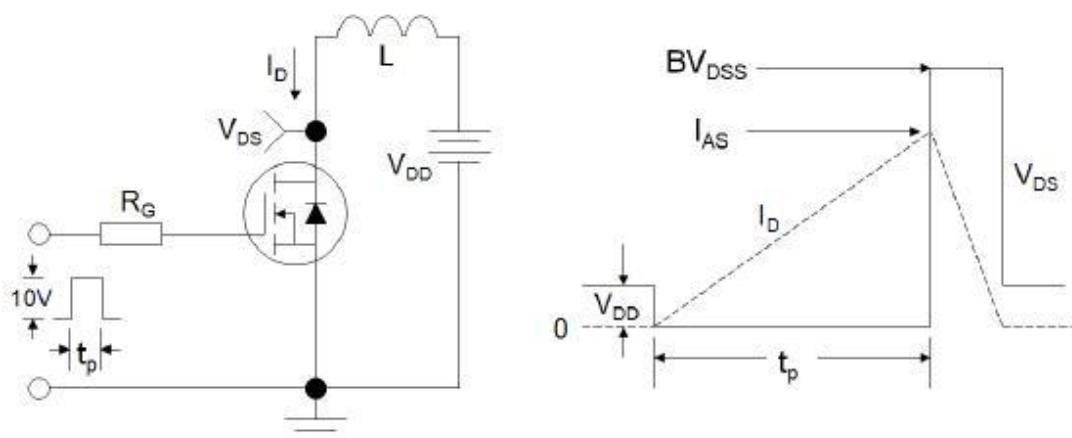
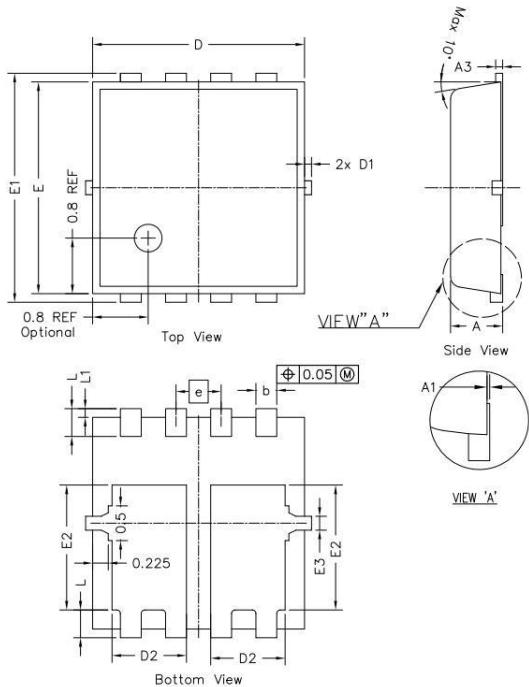


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data- PDFN3x3-8L-D



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
A3	0.144	0.152	0.202	0.006	0.006	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65 BSC			0.026 BSC		
D	2.950	3.050	3.150	0.116	0.120	0.124
E	2.950	3.050	3.150	0.116	0.120	0.124
D1	---	---	0.125	----	----	0.005
E1	3.200	3.300	3.400	0.126	0.130	0.134
D2	0.970	1.070	1.170	0.038	0.042	0.046
E2	1.700	1.800	1.900	0.067	0.071	0.075
E3	0.150	0.200	0.250	0.006	0.008	0.010
L	0.300	0.400	0.500	0.012	0.016	0.020
L1	0.075	0.125	0.175	0.003	0.005	0.007

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