



Description

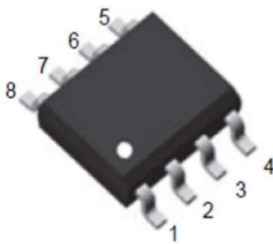
JMT P-channel Enhancement Mode Power MOSFET

Features

- $V_{DS} = -40V$, $I_D = -5A$
 $R_{DS(ON)} < 85m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} < 112m\Omega$ @ $V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

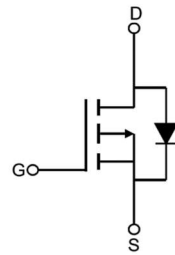
- PWM Applications
- Load Switch
- Power Management



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
850P04A	JMTP850P04A	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	-5
		$T_A = 100^\circ C$	-3.3
I_{DM}	Pulsed Drain Current ^{note1}	-20	A
P_D	Power Dissipation	$T_A = 25^\circ C$	3.7
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	33.8	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} = -10V, I _D = -3A	-	65	85	mΩ
		V _{GS} = -4.5V, I _D = -2A	-	80	112	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} =0V, f=1.0MHz	-	573	-	pF
C _{oss}	Output Capacitance		-	53	-	pF
C _{rss}	Reverse Transfer Capacitance		-	42	-	pF
Q _g	Total Gate Charge	V _{DS} = -20V, I _D = -3A, V _{GS} = -10V	-	7.1	-	nC
Q _{gs}	Gate-Source Charge		-	1.5	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	1.8	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -20V, I _D = -5A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	6.5	-	ns
t _r	Turn-on Rise Time		-	14	-	ns
t _{d(off)}	Turn-off Delay Time		-	34	-	ns
t _f	Turn-off Fall Time		-	18	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-20	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -5A	-	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S = -5A, di/dt=100A/μs	-	23	-	ns
Q _{rr}	Reverse Recovery Charge		-	25.2	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%



Typical Performance Characteristics

Figure 1: Output Characteristics

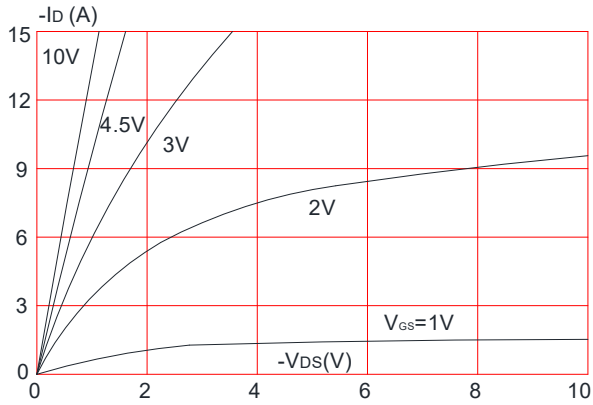


Figure 2: Typical Transfer Characteristics

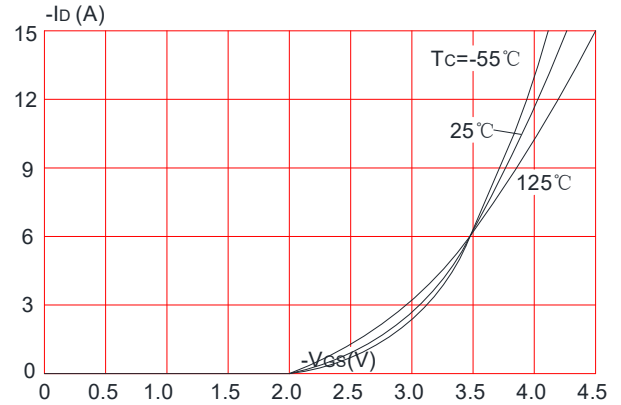


Figure 3: On-resistance vs. Drain Current

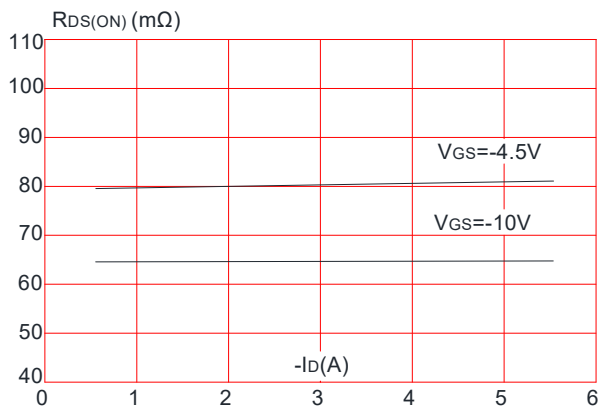


Figure 4: Body Diode Characteristics

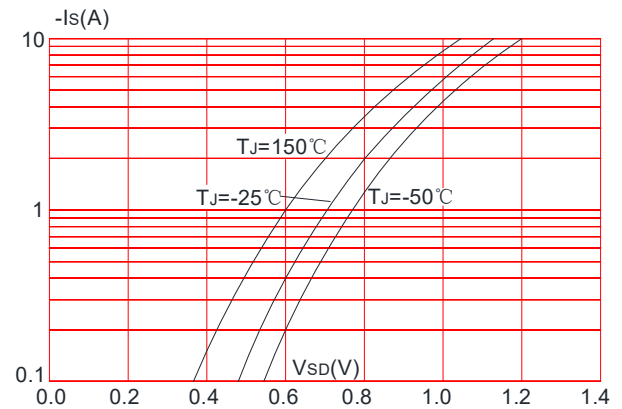


Figure 5: Gate Charge Characteristics

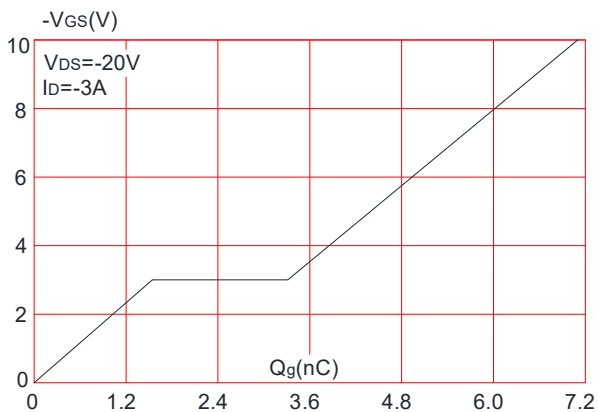


Figure 6: Capacitance Characteristics

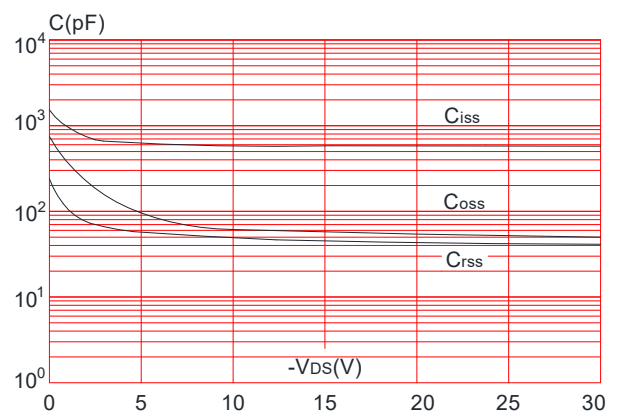




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

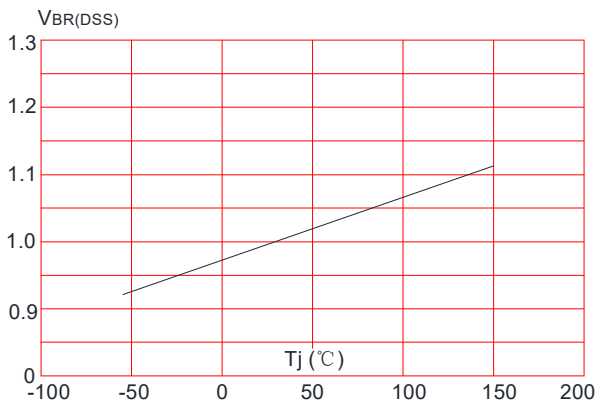


Figure 8: Normalized on Resistance vs. Junction Temperature

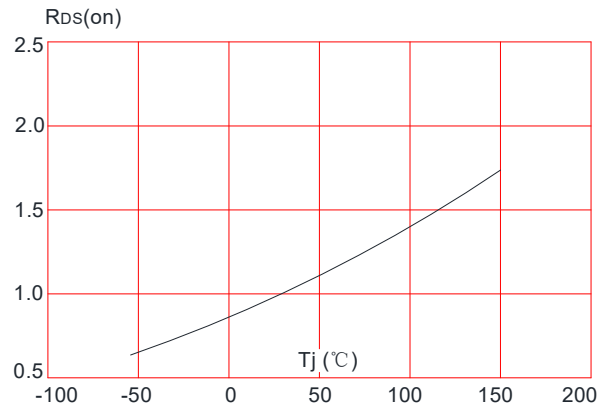


Figure 9: Maximum Safe Operating Area

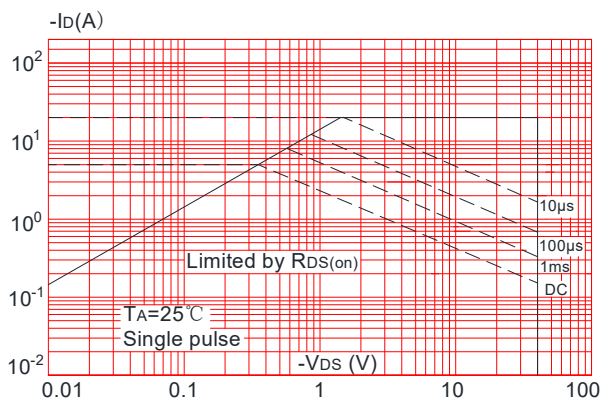


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

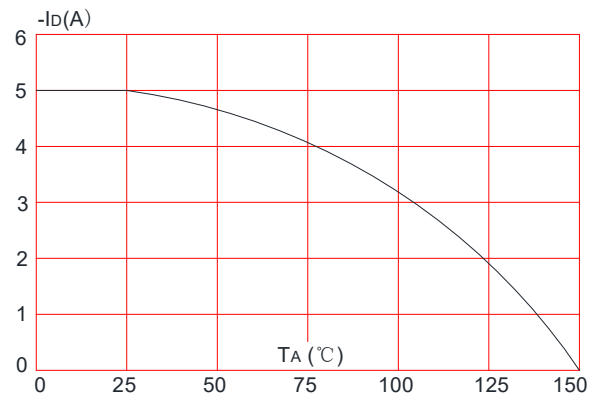
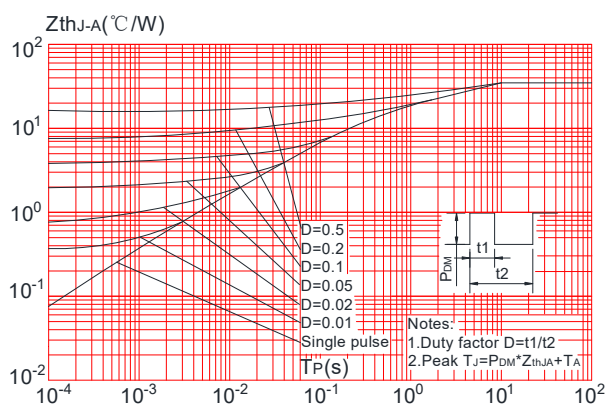
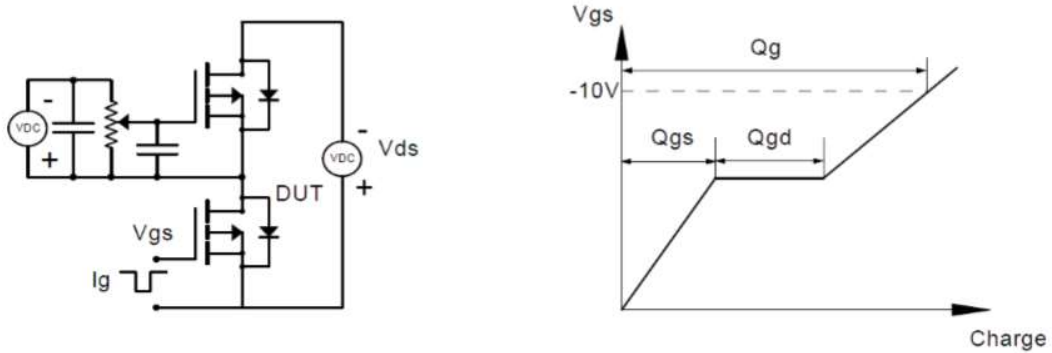


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

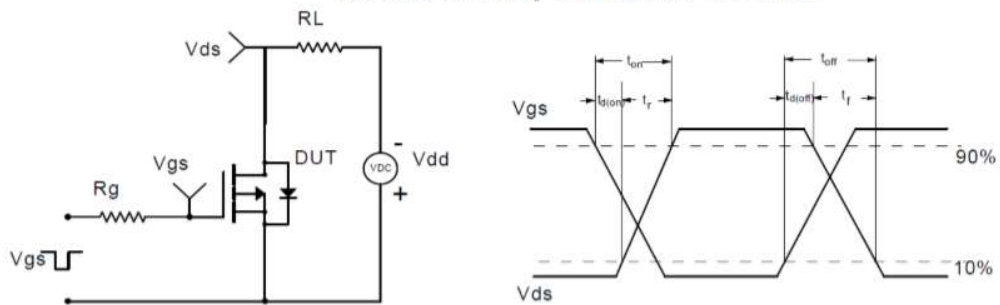


Test Circuit

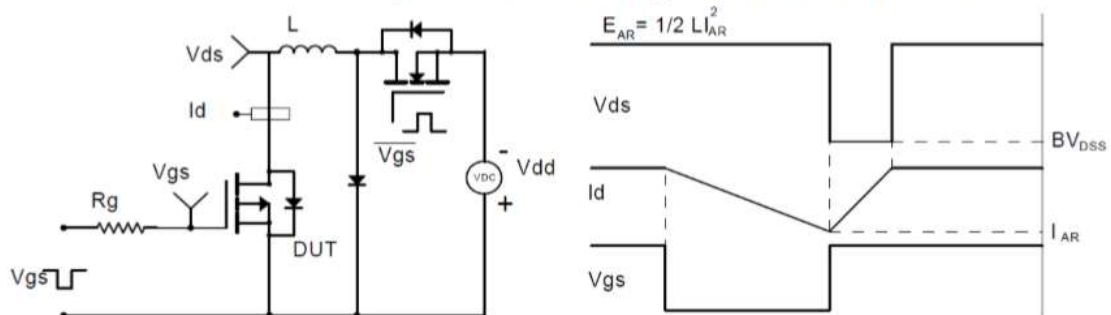
Gate Charge Test Circuit & Waveform



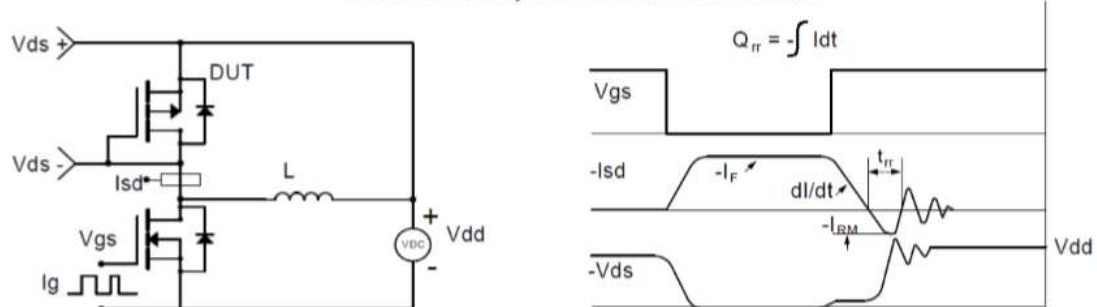
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

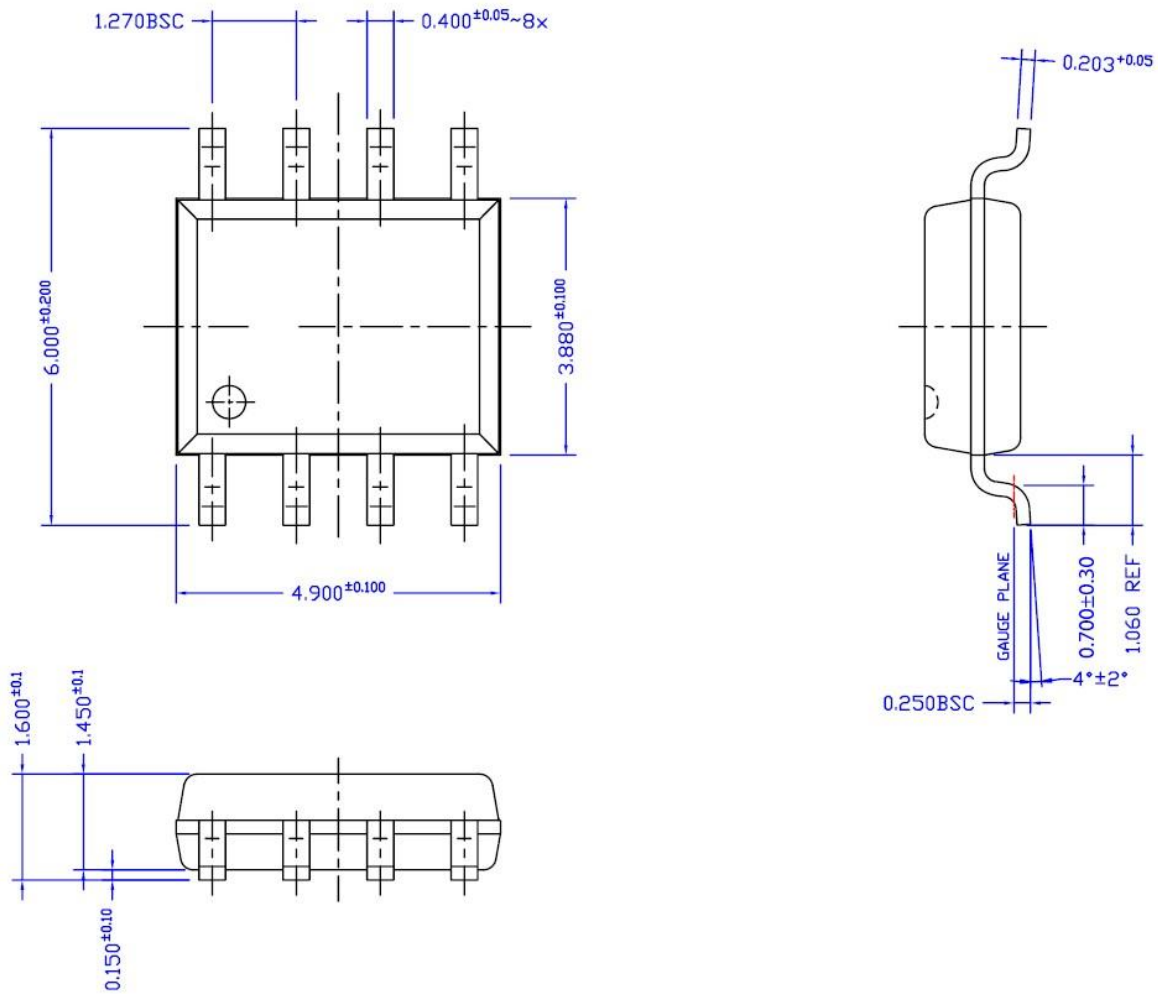


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data-SOP-8



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