



Description

JMT P-channel Enhancement Mode Power MOSFET

Features

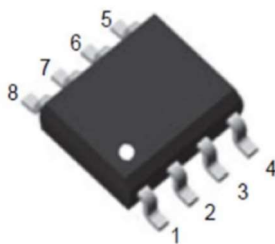
- $V_{DS} = -40V$, $I_D = -40A$
 $R_{DS(ON)} < 14.3m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 22m\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

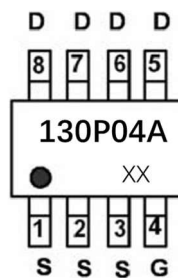
- PWM Applications
- Load Switch
- Power Management



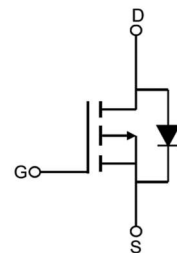
100% UIS TESTED!
100% ΔVds TESTED!



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
130P04A	JMTP130P04A	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	-40
		$T_A = 100^\circ C$	-26
I_{DM}	Pulsed Drain Current ^{note1}	-160	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	144	mJ
P_D	Power Dissipation	40	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	3.1	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.7	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} = -10V, I _D = -20A	-	11	14.3	mΩ
		V _{GS} = -4.5V, I _D = -10A	-	15.5	22	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} =0V, f=1.0MHz	-	3800	-	pF
C _{oss}	Output Capacitance		-	329	-	pF
C _{rss}	Reverse Transfer Capacitance		-	289	-	pF
Q _g	Total Gate Charge	V _{DS} = -20V, I _D = -20A, V _{GS} = -10V	-	42	-	nC
Q _{gs}	Gate-Source Charge		-	7.3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	8.5	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -20V, I _D = -20A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	10	-	ns
t _r	Turn-on Rise Time		-	21	-	ns
t _{d(off)}	Turn-off Delay Time		-	53	-	ns
t _f	Turn-off Fall Time		-	29	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-40	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-160	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -30A	-	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S = -30A, di/dt=100A/μs	-	39	-	ns
Q _{rr}	Reverse Recovery Charge		-	42	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25°C, V_{DD}= -20V, V_G= -10V, L=0.5mH, R_G=25Ω, I_{AS}= -24A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%



Typical Performance Characteristics

Figure 1: Output Characteristics

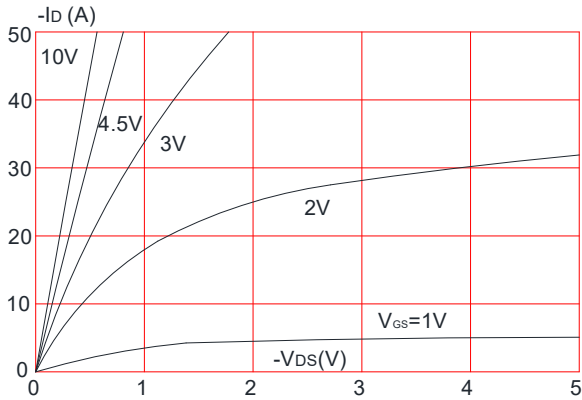


Figure 2: Typical Transfer Characteristics

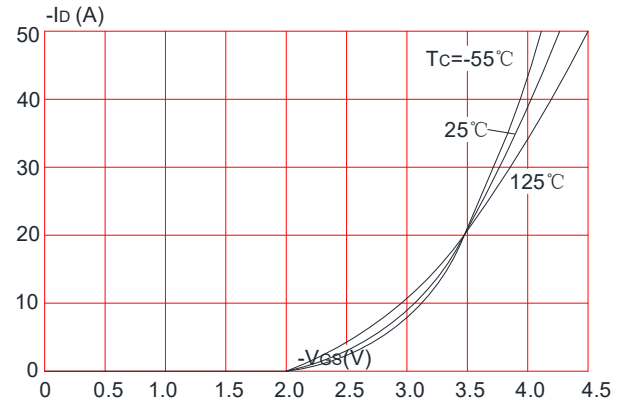


Figure 3: On-resistance vs. Drain Current

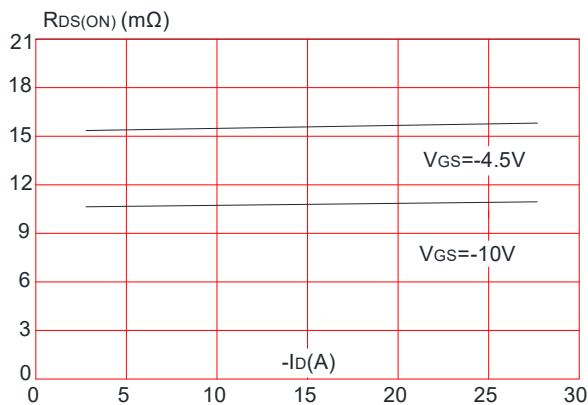


Figure 4: Body Diode Characteristics

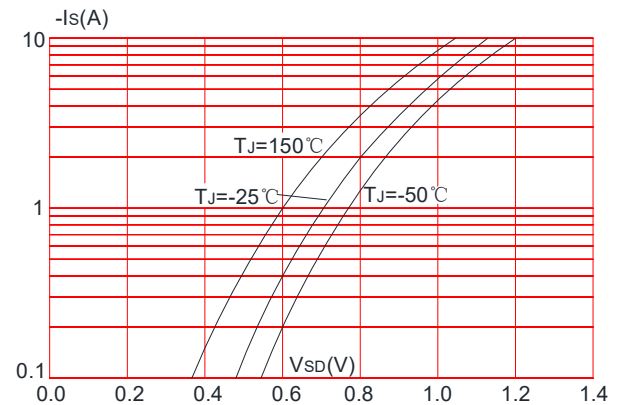


Figure 5: Gate Charge Characteristics

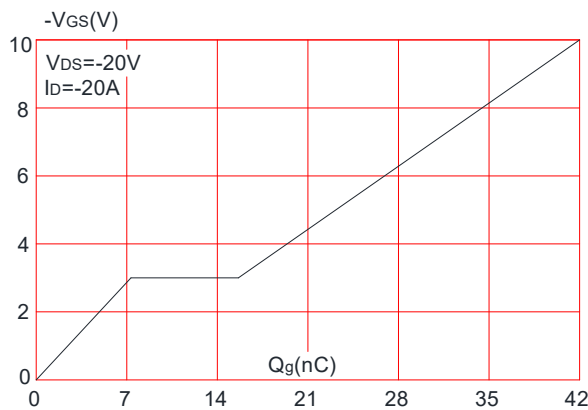


Figure 6: Capacitance Characteristics

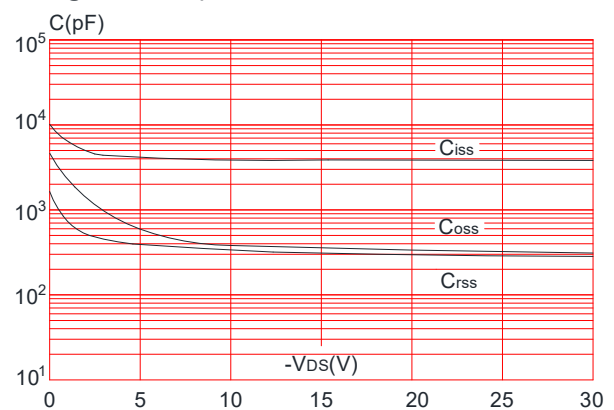




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

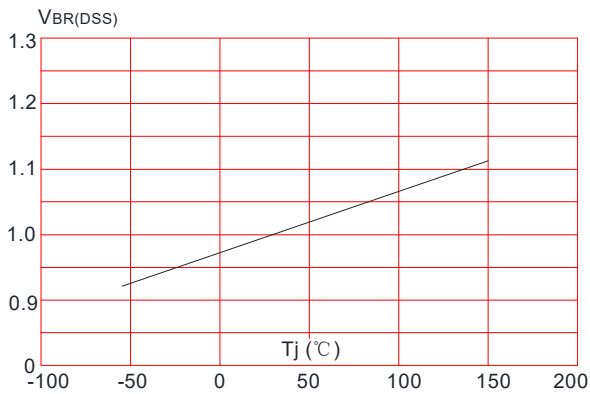


Figure 8: Normalized on Resistance vs. Junction Temperature

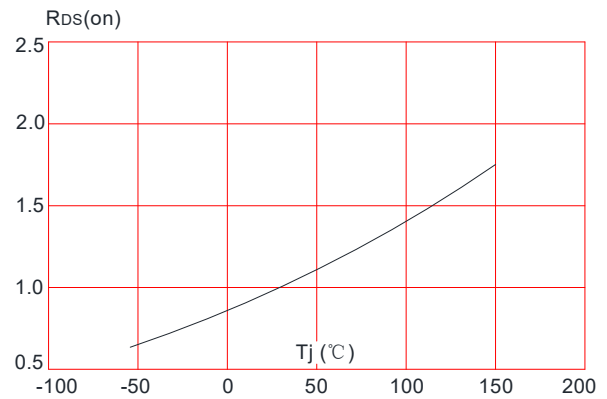


Figure 9: Maximum Safe Operating Area

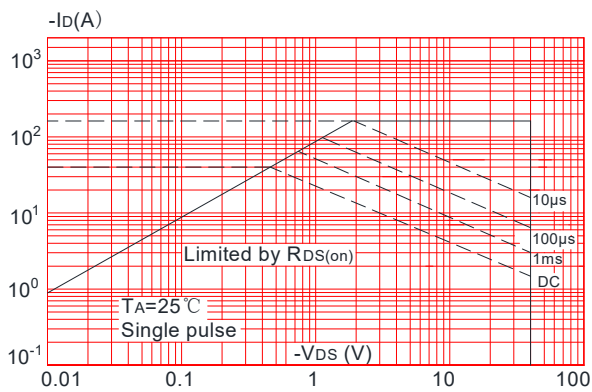


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

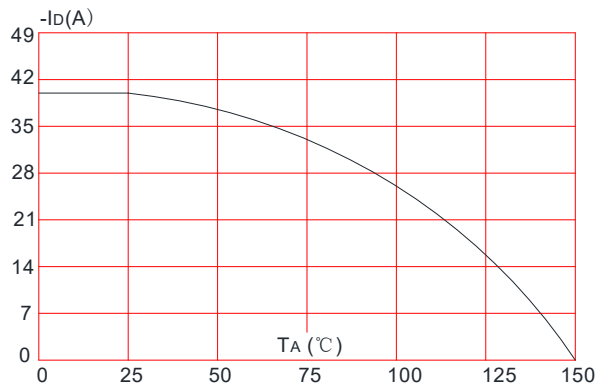
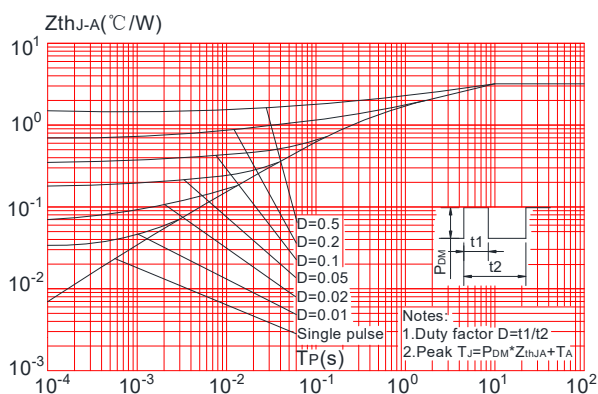
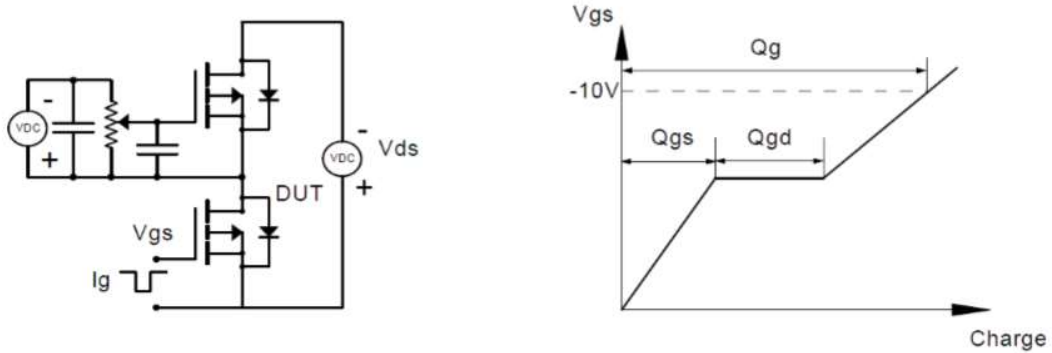


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

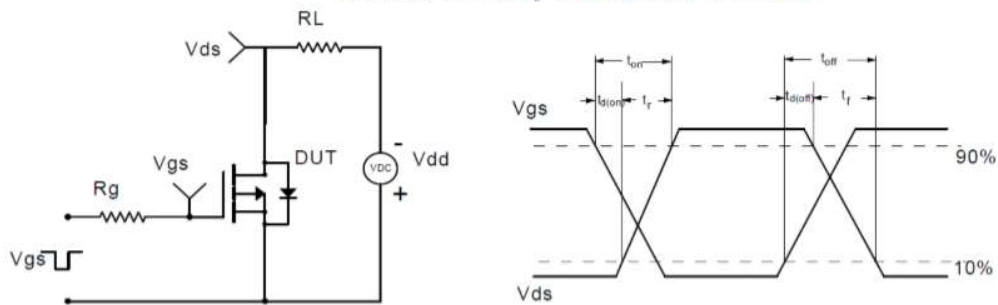


Test Circuit

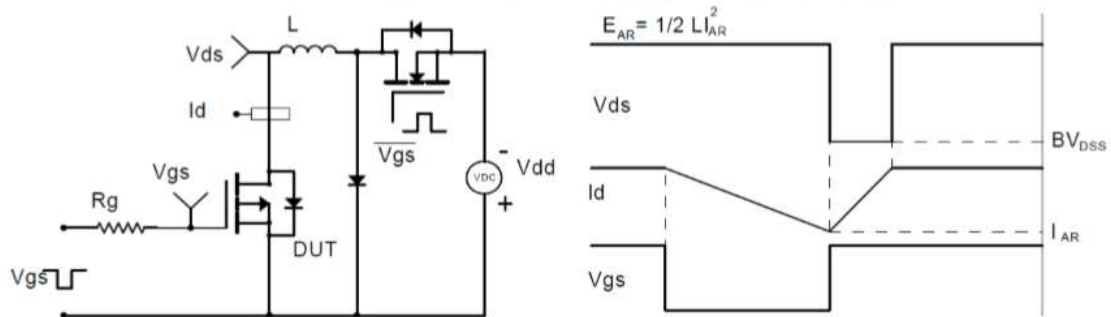
Gate Charge Test Circuit & Waveform



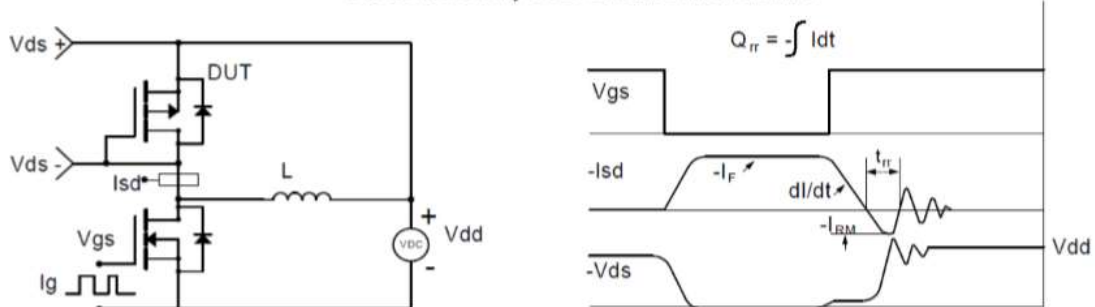
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

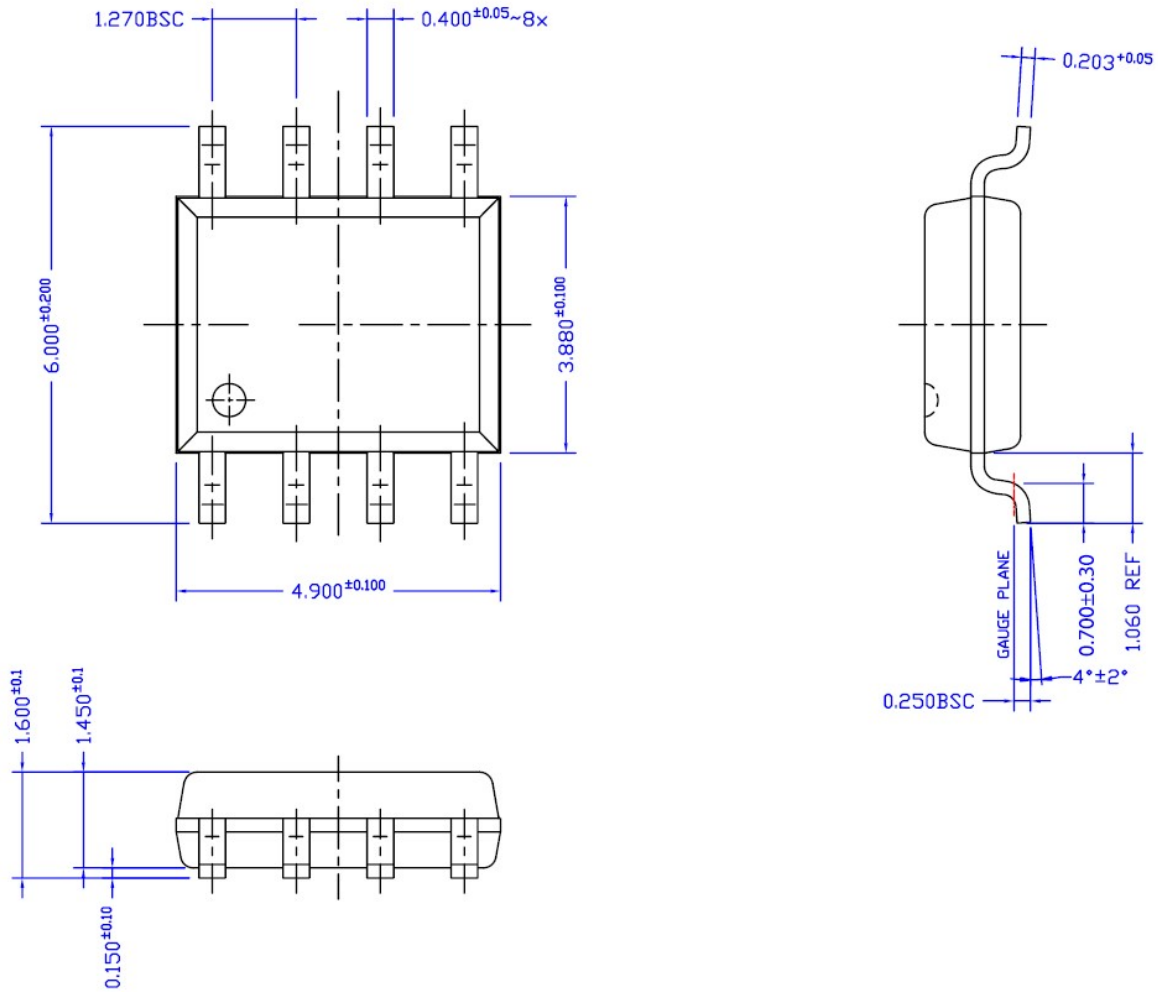


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data-SOP-8



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

This document supersedes and replaces all information previously supplied.



is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

Copyright ©2020 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.