SemiHow
Know-How for Semiconductor

HCD70R1K6
700V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)}$ X Qg)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

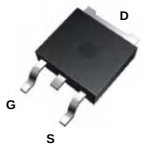
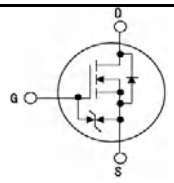
Key Parameters

Parameter	Value	Unit
BV_{DSS} @$T_{j,max}$	750	V
I_D	5	A
$R_{DS(on),\ max}$	1.6	Ω
$Qg_{,\ Typ}$	5.5	nC

Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV Power & LED Lighting Power

Package & Internal Circuit

D-PAK	SYMBOL
	

Absolute Maximum Ratings

T_J=25℃ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	700	V
V_{GS}	Gate-Source Voltage	±20	V
I_D [1)]	Drain Current - Continuous (T_C = 25℃)	5.0	A
	Drain Current - Continuous (T_C = 100℃)	3.2	A
I_{DM} [2)]	Drain Current - Pulsed	8.4	A
E_{AS} [3)]	Single Pulsed Avalanche Energy	43	mJ
I_{AR}	Avalanche Current	1	A
dv/dt	MOSFET dv/dt ruggedness, V_{DS}=0…560V	50	V/ns
dv/dt	Reverse diode dv/dt, V_{DS}=0…560V, I_{DS}≤I_D	15	V/ns
P_D	Power Dissipation (T_C = 25℃)	49	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2500	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	-	2.54	℃/W
$R_{\theta JA}$	Junction-to-Ambient	-	62.5	℃/W

Electrical Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 60 μA	2.5	-	3.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.1 A	-	1.35	1.6	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	700	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 700 V, V_{GS} = 0 V, T_C = 25℃	-	-	1	μA
		V_{DS} = 700 V, V_{GS} = 0 V, T_C = 150℃	-	-	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1.0 MHz	-	245	-	pF
C_{oss}	Output Capacitance		-	13	-	pF
C_{rss}	Reverse Transfer Capacitance		-	1.7	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 350 V, I_D = 1.5 A, R_G = 25 Ω (Note 4,5)	-	20	-	ns
t_r	Turn-On Rise Time		-	18	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	-	ns
t_f	Turn-Off Fall Time		-	20	-	ns
Q_g	Total Gate Charge	V_{DS} = 560 V, I_D = 1.5 A, V_{GS} = 10 V (Note 4,5)	-	5.5	-	nC
Q_{gs}	Gate-Source Charge		-	1.1	-	nC
Q_{gd}	Gate-Drain Charge		-	2.2	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	5.0	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	8.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 5.0 A	-	-	1.3	V
trr	Reverse Recovery Time	V_{GS} = 0 V, I_S = 1.5 A, di_F/dt = 100 A/μs	-	135	-	ns
Qrr	Reverse Recovery Charge		-	0.6	-	μC

Notes :

1. Limited by Tj max. Maximum duty cycle D=0.50
2. Repetitive Rating : Pulse width limited by maximum junction temperature
3. I_{AS}=1A, V_{DD}=50V, R_G=25Ω, Starting T_J =25℃
4. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature

Typical Characteristics

Figure 1. On Region Characteristics

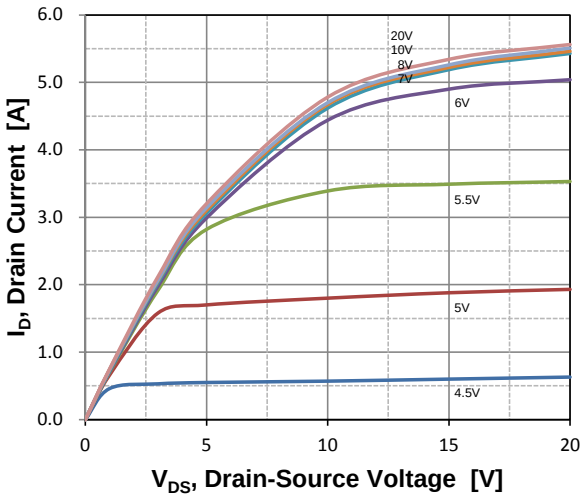


Figure 2. Transfer Characteristics

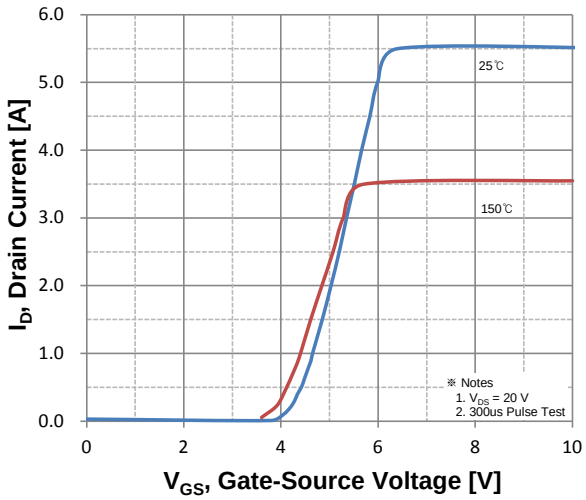


Figure 3. On Resistance Variation vs. Drain Current and Gate Voltage

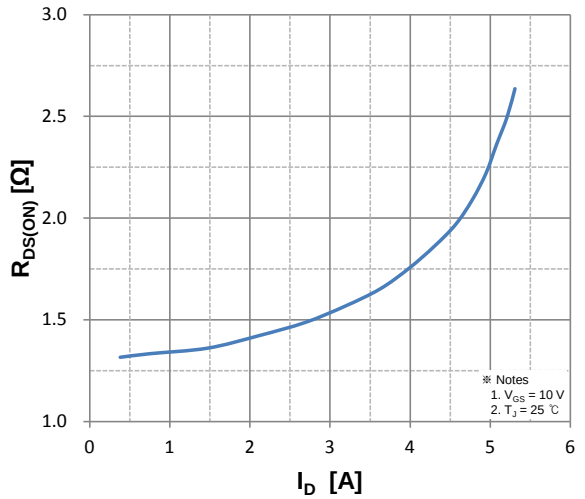


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

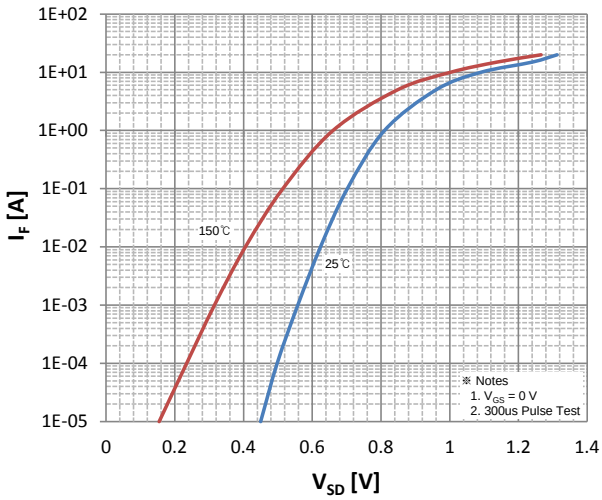


Figure 4. Capacitance Characteristics

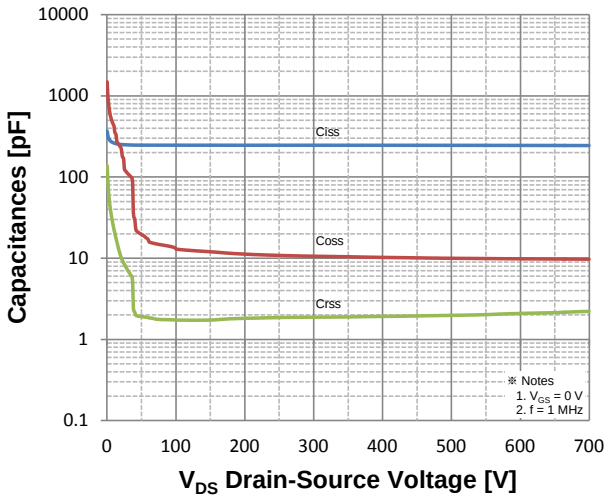
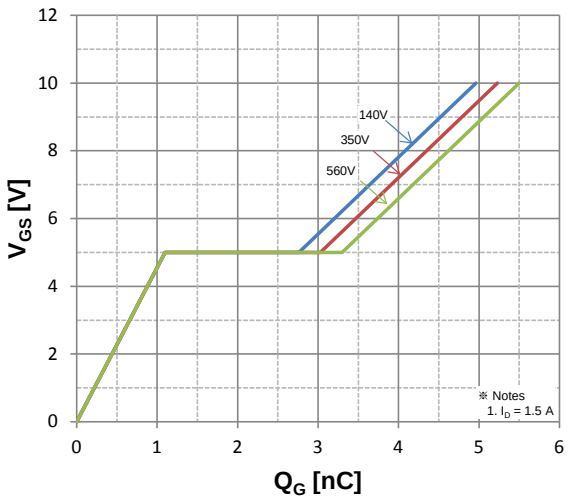


Figure 5. Gate Charge Characteristics



Typical Characteristics

Figure 7. Breakdown Voltage Variation vs. Temperature

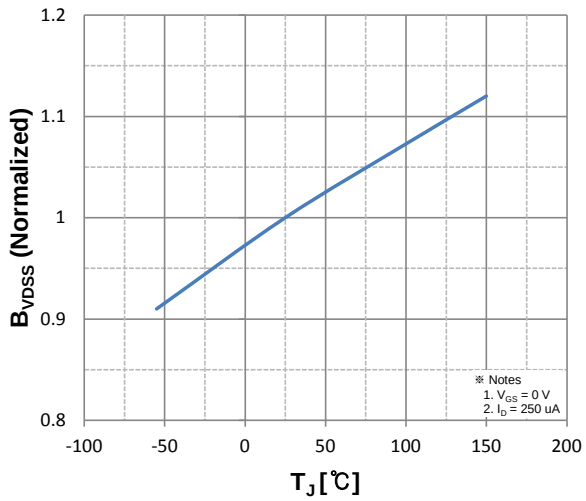


Figure 8. On-Resistance Variation vs. Temperature

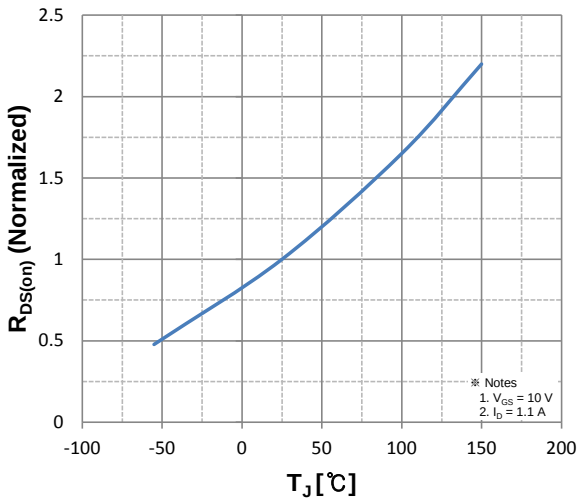


Figure 9. Maximum Safe Operating Area

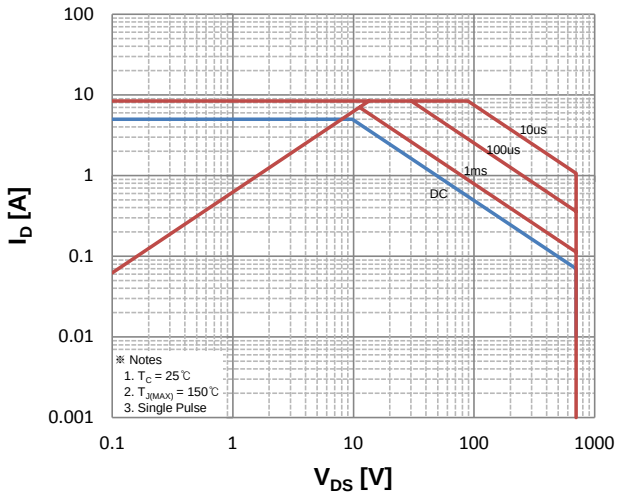


Figure 10. Maximum Drain Current vs. Temperature

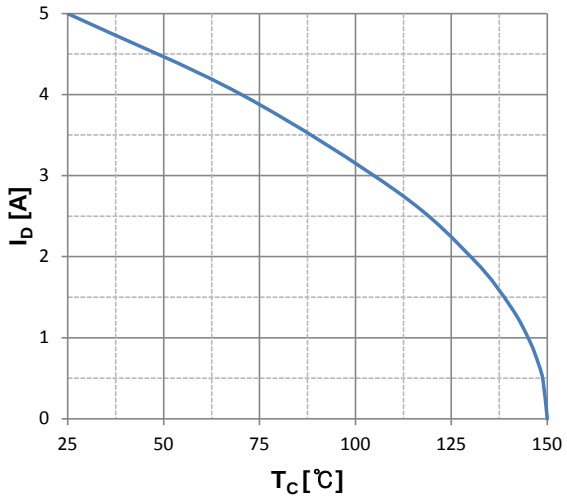


Figure 10. Transient Thermal Response Curve

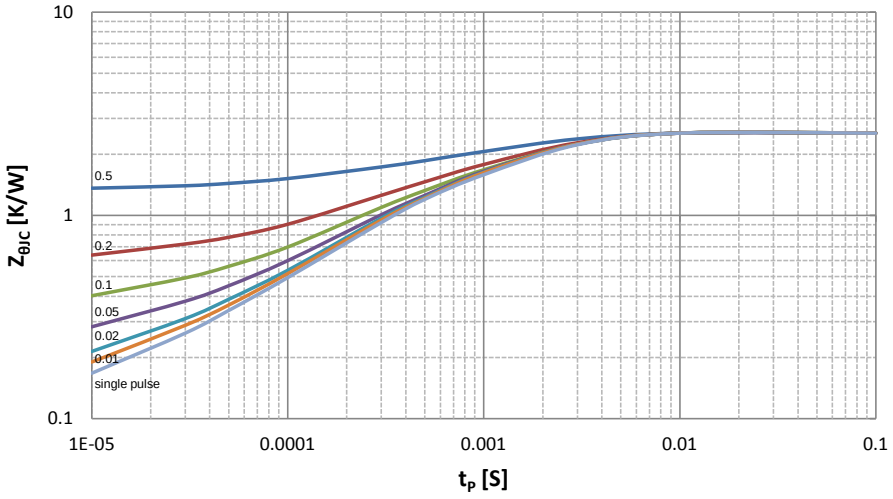


Figure 12. Gate Charge Test Circuit & Waveform

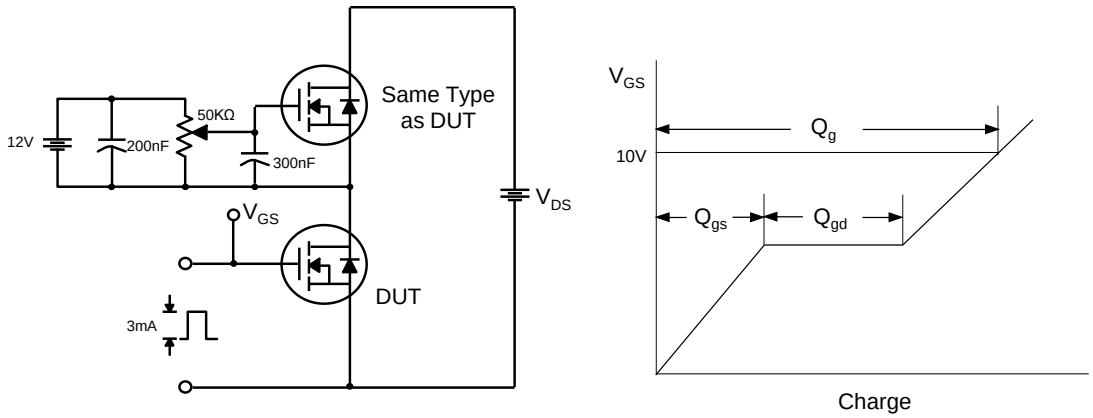


Figure 13. Resistive Switching Test Circuit & Waveforms

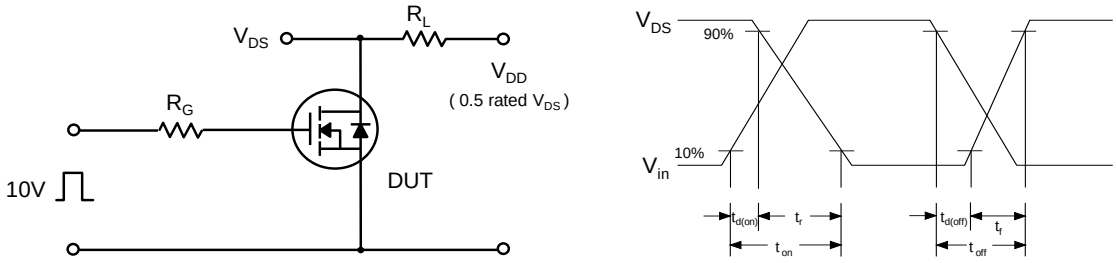


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

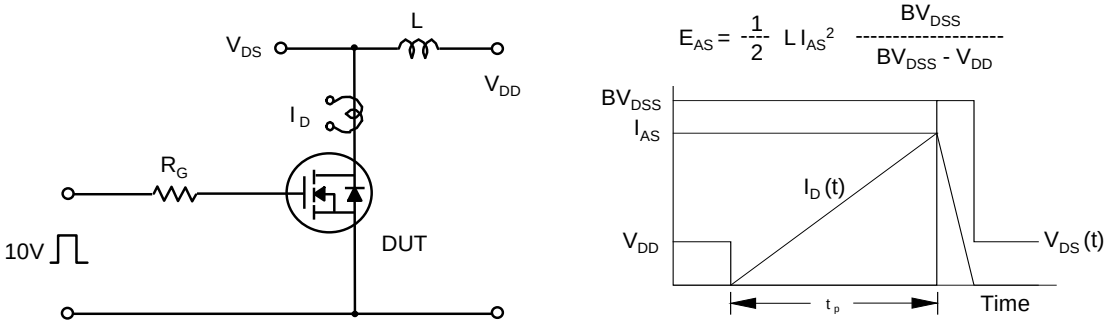
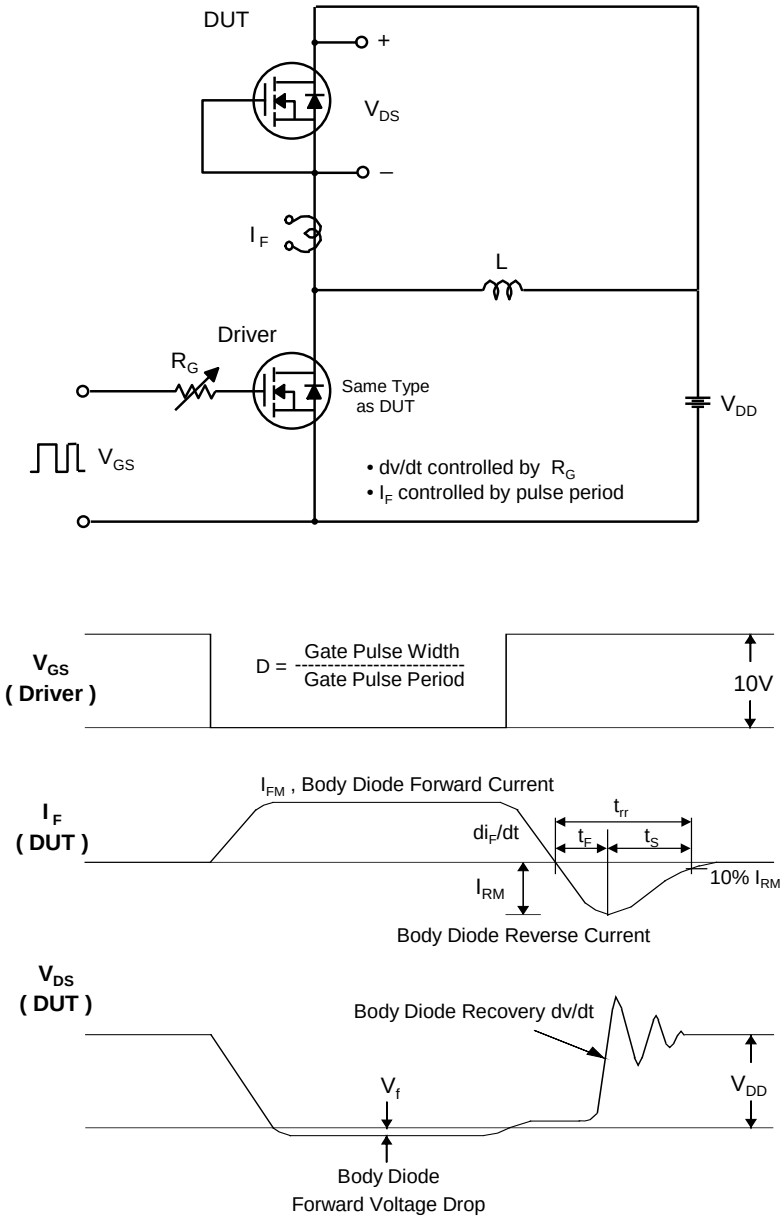


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)